REMARKS

Applicants have amended claim 1 to recite limitations that are inherent in the language of original claim 1. Thus, this amendment does not change actual claim scope.

Claims 1-3 have been rejected under 35 USC 102(b) as anticipated by the Background of the Invention section of the specification. Applicants respectfully traverse this rejection.

Claim 1 recites two different steps of pressure application, i.e., applying a pressure to a peripheral portion of a back surface of the semiconductor chip and applying a pressure to a central portion of the back surface of the semiconductor chip. Because of this two-step pressure application, the claimed manufacturing method prevents the sealing resin from penetrating into the space between the claimed first and second electrodes. See, for example, page 5, lines 12-17, of the specification. The Examiner contends that the conventional pressure application to the whole back surface of the semiconductor chip through the movable plate 8, which is explained at page 1, line 22 - page 2, line 6, of the specification and shown in FIG. 3B of the application, corresponds to the claimed two-step pressure application.

Applicants respectfully disagree with the Examiner. Claim 1 recites two different pressure application steps as explained above, while the conventional pressure application shown in FIG. 3B applies pressure simultaneously to the peripheral and central portions of the back surface of the semiconductor chip. However, for the Examiner to understand the claimed invention properly, applicants have added to claim 1 a statement of what was inherent in the claimed two-step pressure application so as to recite applying, after the application of the pressure to the peripheral portion, a pressure to a central portion of the back surface of the semiconductor chip so that the sealing resin extends in a space between the substrate and the front surface of the semiconductor chip. Because the conventional pressure application shown in FIG. 3A applies the pressure to the central portion of the back surface of the semiconductor chip at the same time as it applies the pressure to the peripheral portion, the conventional pressure

application does not apply the pressure to the central portion after the application of the pressure to the peripheral portion as claimed.

Thus, the rejection of claims 1-3 under 35 USC 102(b) as anticipated by the Background section should be withdrawn because the Background section does not teach or suggest the claimed application of the pressure to the central portion of the semiconductor chip after the application of the pressure to its peripheral portion.

Claims 1-7 have been rejected under 35 USC 102(e) as anticipated by U.S. Patent No. 6,674,178 (Ikegami). Applicants respectfully traverse this rejection.

Even though the Examiner rejects claims 1 and 4 in this anticipation rejection, the Examiner applies Ikegami only to the invention of claim 4 and provides no reasons why Ikegami anticipates claim 1. Claim 1 recites the application of the pressure to the central portion of the semiconductor chip after the application of the pressure to its peripheral portion, as explained above. Ikegami's method includes holding semiconductor chip 11 by vacuum holding collet 24 and hot-pressing the semiconductor chip 11 to interconnection board 14 with resin 17. See, for example, column 8, line 38 - column 9, line 22, of Ikegami. Thus, Ikegami's method first applies a pressure, i.e., a negative pressure for suction to hold the semiconductor chip 11, and then applies a pressure to the peripheral portion of the semiconductor chip 11 held by the vacuum holding collet 24 for attaching the chip 11 to the board 14. No part of Ikegami teaches or suggests that a pressure, either suction or compression, be applied to the central portion after an application of a pressure to the peripheral portion as claimed.

Claim 4 recites applying a negative pressure to a central portion of a back surface of the semiconductor chip and a positive pressure to a peripheral portion of the back surface of the semiconductor chip so that the first and second electrodes come into a contact, and applying a positive pressure to the central portion of the back surface of the semiconductor chip so that the sealing resin extends in a space between the substrate and the front surface of the semiconductor chip. The Examiner contends that the Ikegami's vacuum holding collet 24 explained above

corresponds to the first pressure application step of claim 4 because the vacuum collet 24 applies a sucking pressure to the central portion of the semiconductor chip 11 through suction hole 24a while other area of the vacuum collet 24 applies "a fixed amount of force" to the semiconductor chip excluding the central portion. See paragraph 2 of the Action. Applicants do not disagree with the Examiner with respect to this finding.

The Examiner then contends that column 8, lines 24-43, of Ikegami discloses the claimed application of the positive pressure to the central portion of the semiconductor chip. Applicants respectfully disagree with the Examiner. The cited portion of Ikegami only explains the effect of the application of the "fixed amount of force" to the peripheral portion of the semiconductor chip. Neither the cited portion of Ikegami nor any other portion of Ikegami teaches or suggests that a positive pressure be applied to the central portion in addition to the application of the negative pressure to the central portion and the positive pressure to the peripheral portion. Furthermore, persons of ordinary skill in the art would have understood that Ikegami's negative pressure applied to the central portion of the semiconductor chip for suction holding must be maintained while the positive pressure is applied to the peripheral portion of the semiconductor ship because otherwise the semiconductor chip might shift under the application of the positive pressure. Thus, Ikegami's vacuum holding collect 24 cannot apply a positive pressure to the central portion of the semiconductor chip as claimed, and Ikegami discloses no other means to apply pressure to the semiconductor chip.

The rejection of claims 1-7 under 35 USC 102(e) on Ikegami should be withdrawn because Ikegami does not teach or suggest the claimed two-step pressure application.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **492322017800**.

Respectfully submitted,

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